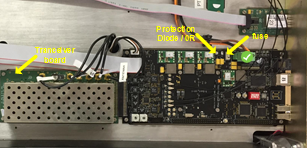
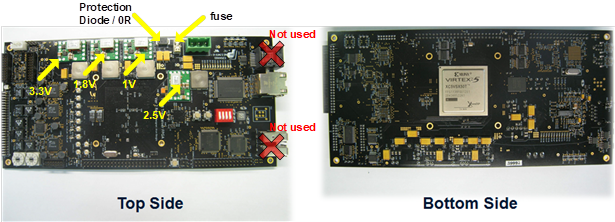
**Step 8: Testing the FPGA & RF Transceiver Boards** (Labels in Figure 21 & 22)

1. Connect Phoenix connector J4 to the Power Distribution Board.
2. Remove STC and connect the ribbon cable from the FPGA to the PDB on P2 as well as on the FP on P2.
3. This will provide power and signals to the FPGA board and the RF Transceiver Board.
4. Turn on the mains and FP.
5. Check that you are getting 5V (brown wire) and 15V (orange wire) on J4 supplying the FPGA.
6. BEFORE GOING ON MAKE SURE THAT ALL CONNECTIONS ARE CORRECT, ALL CABLES ARE SECURE AND THERE ARE NO LOOSE PARTS ON THIS SIDE OF THE BOARD.
7. Disconnect any cables and turn over the box.
8. **D1** on the Lantronix board should light up if all is OK. (**Figure 9**)
9. Check the address screen for the Lantronix (Figure 9)
10. The FPGA Board has its own power regulation for all the different supply voltages it requires.
11. The easiest way to check that these are all in order is to look on the Voltage Screen on the Front Panel.
12. You can also check LED’s D9, D10, D11, D12 & D13.
    * Fault finding will be difficult but try and check the DC-DC converter modules if there is a problem with one of the voltages. For example, 1.8V is mostly limited to the 1GIG Ethernet controller (Lantronix), so check there if there is an issue with 1.8V (this fault has happened before).
    * NOTE the 1.8V is hard coded into the Front Panel, so if weird things are happening with the FPGA please manually check it on the FPGA.
13. The FPGA has a known problem where it starts to brown out due to the voltage drop across the fuse and the reverse protection diode being too high. The fuses have been replaced with 4A fuses and the diodes have been replaced with 0R resistors. Any FPGA without these modifications are susceptible to this problem and should receive the modification.



**Figure 21:**

**Testing the FGPA & RF Transceiver Boards (Top Side).**

****

**Figure 22: Top and Bottom views of the FPGA board**

**Step 9: (Transceiver Board)**

Make sure that the oscilloscope is setup to trigger on the channel being used to measure and test on!

And ZOOM in on the oscilloscope (channel 2 at 50 Ω) as the signals being measured in this test are mostly all very small.

If you find a fault during these steps please have a look at the end of this step.

1. Disconnect the transceiver board from the FPGA and remove it from the box.
2. Connect the transceiver board to the “RF Transceiver Test Board Ver 1.2” and power this setup with an external 15 V from a bench power supply.
3. Switch the power on and make sure all 4 power LEDs on the tester board light up; and that each LED corresponding to a DIP switch, is on when the dip switch is turned on.
4. Switch all dip switches off again and cycle power.
5. Switch on the AWG and set the frequency to 12.5 MHz and set the amplitude to 100mVp-p.
6. Connect the output of the AWG to the DAC2 port and observe the signal as output on DAC2\_OUT, you should see around 90 to 100mV pk-pk.

(nearly there may be small losses you should see at least around 97mV)

1. Connect the output of the AWG to the DAC1(Tx) port and observe a signal with an amplitude of ± 25 mV pk-pk on Tx\_OUT.
2. Flip the TxAGC (LE) switch on and observe a signal with an amplitude of ± 800 mV pk-pk on Tx\_OUT.
3. Flip the other TxAGC (1dB – 16dB) switches on one by one and observe an increasing attenuation of the signal on Tx\_OUT, corresponding to flipping the switches of increasing dBs.
4. Connect the output of the AWG to the Antenna port on the transceiver board and observe the same signal as output on MON2.
   1. (+- 90mV)
5. Connect the output of the AWG to the Current port and terminate the PwrAmp port; observe a signal with an amplitude of ± 62 mV pk-pk on MON1.
6. Flip SWB switch on and observe the signal on MON1 turn off.
7. Switch the power off and swap the inputs to the Current and Pwr\_Amp ports.
8. Switch the power back on and verify once more a signal with an amplitude of ± 95 mV pk-pk on MON1.
9. Flip SWB switch off and observe the signal on MON1 disappear.
10. Flip SWB switch on and back off again, watching the signal with an amplitude ± 95 mV pk-pk re-appear and disappear again on MON1.
11. Power off and change the AWG output from 100 mV pk-pk to 1 mV pk-pk.
12. Connect the output of the AWG to the RFin port, unterminated Current and terminate the DAC1(Tx) port.
13. Observe a 20mV pk-pk output signal output on ADC(Rx).
14. Power on
15. Flip the RxAGC (LE) switch on, observe a signal with an amplitude of ± 800 mV pk-pk on ADC(Rx).
16. Flip the other RxAGC (1dB – 16dB) switches on one by one and observe an increasing attenuation of the signal on ADC(Rx), corresponding to flipping the switches of increasing dBs.

IF you have a fault please check the following:

* Open faraday casing on transceiver board to access the below pins.
* Power the setup with the 15V supply and check:
  + 1. Pin 20 is +- 10.5V
    2. Pin 19 is +- 3.3V

These boards cannot be fixed here at SANAE 4 so please MARK **CLEARLY** and make sure it gets sent back to SANSA and a new one is ordered.

1. Put the board back and all RF connectors.
2. Tighten or check the phoenix connectors and mounting screws on this side of the box.
3. SET THE CORRECT BOX NUMBER ON THE FPGA’ selector switches
   1. The closest switch to the LAN ports is the least significant decimal.
   2. The closest to the front is the most significant decimal.

**Step 10: Transceiver box operation test and calibration**

* Flip the box for the final stage.
* Setup transceiver box with timing box, oscilloscope and computer as shown in the figure below.

TxRx Box

Computer

Switch

Oscilloscope

Timing Box

TxRx

Antenna Output HV Probe !

Timing ( green cable )

FPGA

LANtronix

FPGA (Grey Cable)

LANtronix ( Red cable )

Ethernet

Ethernet

Transmit and Receive test:

* Ensure all cables are plugged in; And the dummy load is connected to the antenna port
* High voltage Probe, channel 4 on the Antenna output pint on the filter board.
* The TxRx on the PWRAMP connected to channel 1.
* On the computer (Joshua) go to /T3/cpart/ [*Run command: cd /T3/cpart/]*

TRANSMIT TEST

* Ensure that there are 2 boxes alive (Timing box and Transceiver box being tested)
* Run ./sop
* **ENSURE DUMMY LOAD IS CONNECTED!!!**
* Enter 1 for transmit test, then 3 to transmit
* You should hear the box switching and see the TxRx signal as well as the antenna output (500Vp-p) on the oscilloscope and check that the count is increasing on the front panel.
* To stop the test, enter 5
* Run ./sop and then press cntl + c to reset the box.

RECEIVE TEST **MAKE SURE TO PRESS 0 AND NOT 1 WHEN YOU RUN SOP !!!!!**

* For the receive test, replace the dummy load with AWG set to 9.999 980MHz @ 1mVp-p
* DISCONNECT the signal generator cable from the actual machine, this is an extra safety to make sure you DON’T break the signal generator.
* Run ./sop again and enter 0, then 3 to begin the transmit. (yes it says transmit but you are actually receiving)
* Once you see a graph outputting on the PC screen, then attach the signal generator and the turn on the output.
* This is again to make 100% sure you are not going to pump 1000V into the signal generator.
* When you switch on the AWG you should see a waveform on the computer with amplitude around 30 000 peak-to-peak
* To stop the test, enter 5.
* Run ./sop and then press cntl + c to reset the box.

Calibration:

* For the calibration, **replace the AWG input with the dummy load.**
* MAKE SURE YOU HAVE REPLACED THE AWG WITH A DUMMY LOAD !!!
* Run ./sop and enter 1, then 3 to transmit.
* Wait for the signal to grow fully on the oscilloscope.
* Once you hear the switching, press 4 to enter calibration
* Enter the box node number you wish to calibrate
* Once calibration is complete, run ./sop and then press cntl + c to reset the box and do another transmit test to confirm antenna output is 500Vp-p

**STEP 11: Final Test for the Front panel and FPGA voltages**

1. This is the final test for the FPGA voltages, look at the Front panel.
2. You have all ribbon cables and Phonex connector plugged in.
3. Power the mains and the FP.
4. Scroll using the turn knob to the voltage screen on the Front Panel and check that the voltages are displaying.

* If any voltages from the Power Distribution Board or FPGA are missing check the ribbon cable.
* Remember that you CAN’T now apply the 3.3V via the STC to the PDB as the FPGA is attached so you will NOT see 50V or High voltage, check those when you do the transmission test. ( next step )
* Voltage labels and what they should be :

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| PHV |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| P50V |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| P15V |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Cur |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| P5V |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| P3V3 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F3V3 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 2V5 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1V8 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1V0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

NOTE : The 1V8 read out is hardcoded into the screen display, this is because there are not enough pins to read the voltage, this number will never change.

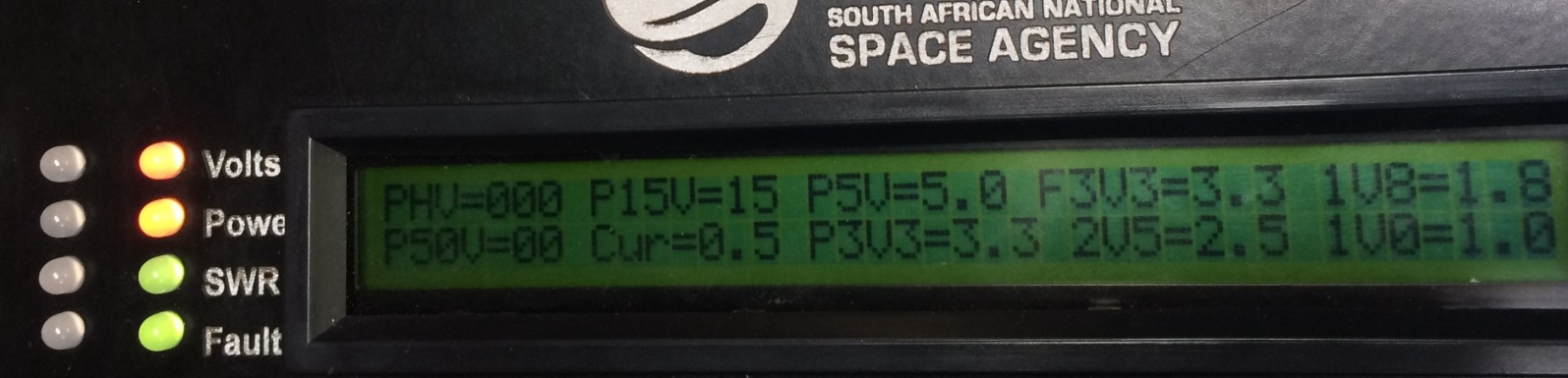


Figure 23 : Front Panel LCD Voltage display

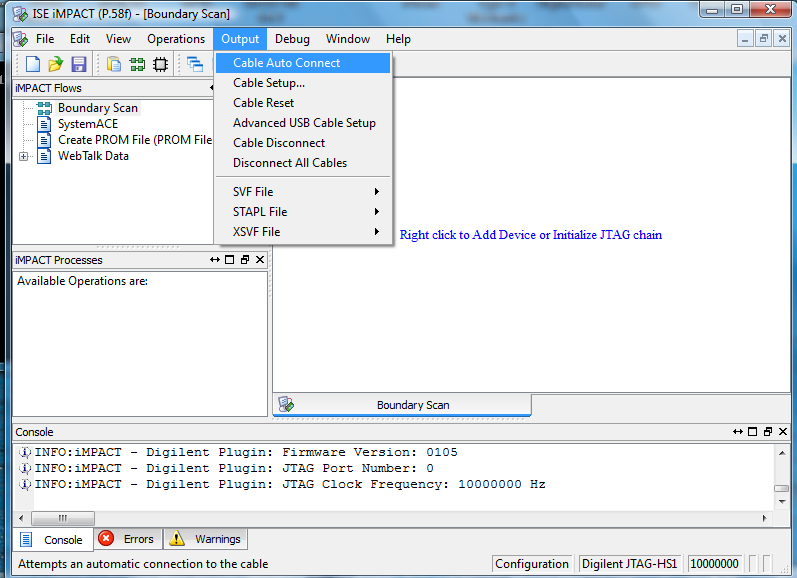
**Programming the FPGA**

\*\*\*NOTE: If the FPGA is new and empty (it will be flashing all its lights when switched on); you have to programme it for the first time via JTAG emulator, following the steps described below. If the FPGA is however not empty and has been programmed before; the ethernet connection to the radar server and a simple programme can be used to re-program the flash of the FPGA. In the home directory (/home/radar/) the programme can be found under T3/nflash/. When you are in the correct directory (/home/radar/T3/nflash), run the following command: *“./fpgaflash all*”

**NB: SWITCH OFF TIMING BOX FIRST!!!**

**Programming the FPGA via JTAG emulator:**

1. Plug in your USB programming cable
2. Plug the JTAG part of the programming cable into the FPGA board and power up the transceiver box.
3. Open iMPACT 64 bit (Xilinx Design Tools/Lab Tools/iMPACT 64-bit) and close any windows that automatically open.
4. In the *Flows* window on the left panel, double click *Boundry Scan*
5. In the *Output* menuk click *Cable Auto Connect*



1. Check that the programming cable is detected by looking in the status bar in the bottom right.
2. Click the *File* menu and choose *Initialise Chain (Ctrl +I)*

\*\*\*ALTERNATE STEPS TO FOLLOW STEP 7:

7.a. If prompted about a config file, say yes.

7.b. Browse to and select: */Digital Radar/Transceiver boxes/FPGA/Code/V2\_Test\_Sx.bit*

7.c. When asked: *Do you want to attach flash?*; click *Yes.*

7.d. Browse to and select: */Digital Radar/Transceiver boxes/FPGA/Code/test.mcs*

7.e. Select the right settings:

BPI PROM: 28F128J3D

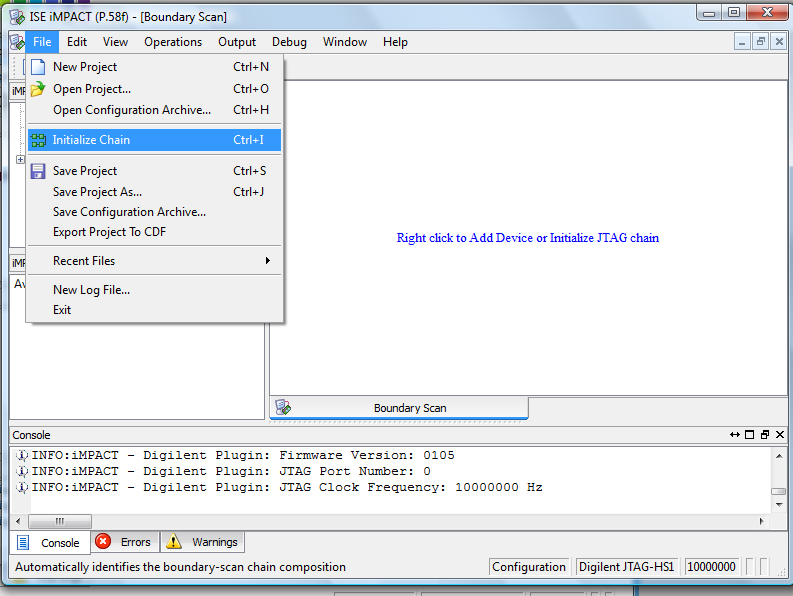
Data Width: 16

Select RS[1:0]b Pin Address Bits: NOT USED

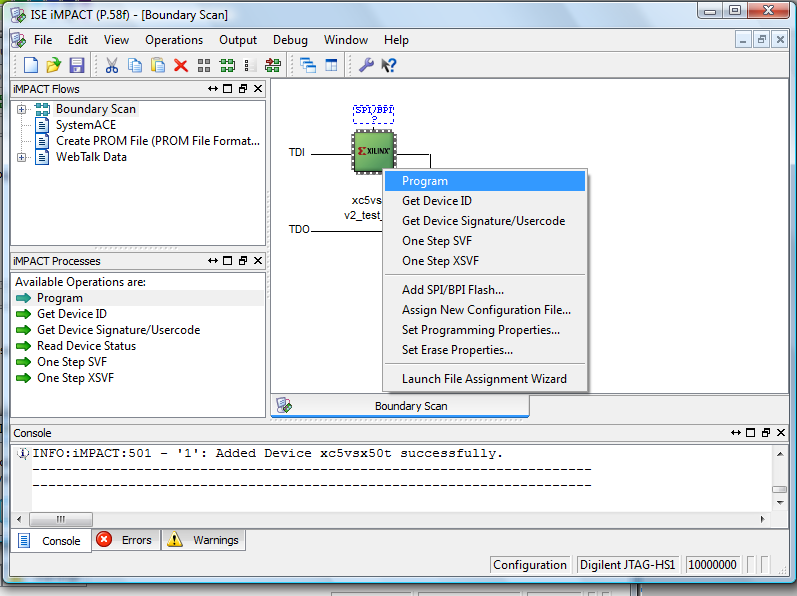
7.f. Right click on FPGA; then click Program.

7.g. Right click on Flash; then click Program. (This step takes quite a while to complete!)

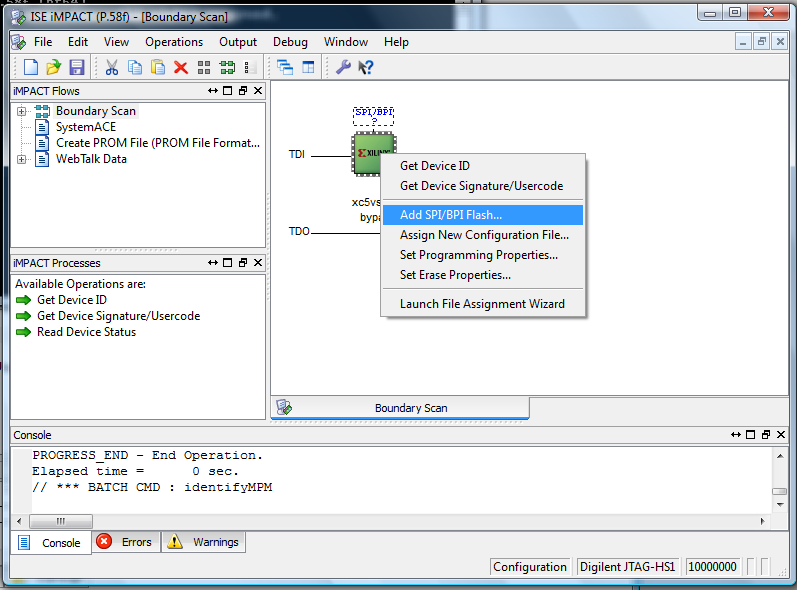
(If pop-ups come up in steps f and g; click on OK.)



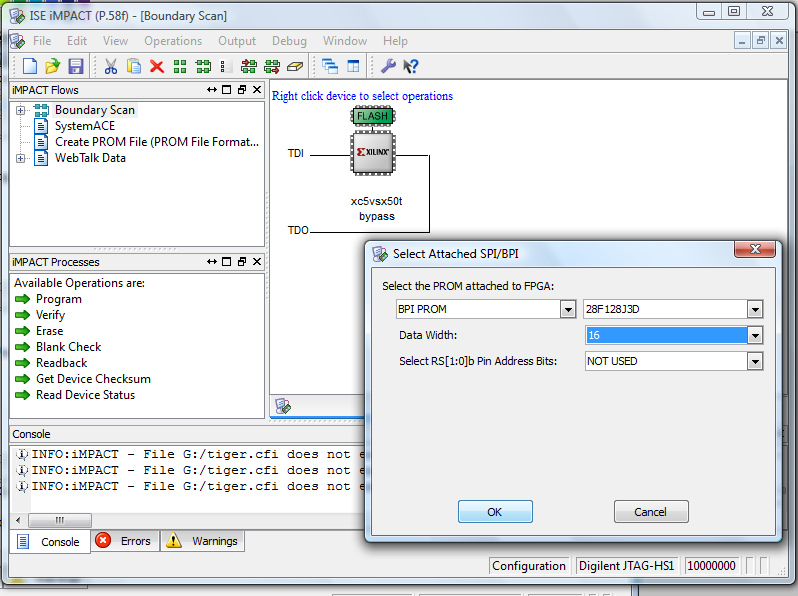
1. A device will appear and you will be prompted to select a *bit* file. You can choose the*bit* file or click cancel/bypass if you just want to programme the PROM.
2. If you selected a *bit* file you can choose *NO,* when asked if you want to add an SPI or PROM.
3. Click OK to close the next pop-up window.
4. Now you can double click on *Program* in the *Process Window* or right-click on the device and choose *Program*



1. If you chose to bypass the *bit* file then you need to add a PROM
2. Right-click on the device and choose *Add SPI/BPI Flash...*



1. Select your *MCS* file and then choose the settings as shown in the Figure below and then press *OKAY.*



1. Right click on the *FLASH* device and choose *Program.*
2. The process will take several minutes to complete. Don’t worry if it gives you a CPI warning.

